30nm Physical Gate Length CMOS Transistors with 1.0 ps n-MOS and 1.7 ps p-MOS Gate Delays

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Components Research

Intel Corporation

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Introduction

- 70nm logic generation in production 2005
  - Transistor physical L_{GATE} ~ 35nm
  - Transistor research for 70nm technology node in progress
- Are conventional planar CMOS transistors scalable to the 70nm technology node ?
  - Short channel effect
  - Device performance
  - Junction edge leakage

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Objective of Work

- **Fabricate and evaluate conventional planar CMOS transistors for the 70nm technology node**
  - **Standard device architecture and process flow**
  - **30nm physical gate length**
  - **0.8nm physical gate oxide thickness**
  - **V_{DD} = 0.85V**

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Experimental Process

- 248nm phase shift mask lithography to form 30nm polySi lines
  - Special processing to form photo-resist lines with > 10:1 height-to-width aspect ratio
- 0.8nm gate oxide
- Aggressively scaled polySi gate and junctions
  - Height of polySi gate electrode < 60nm
  - Rapid thermal anneal temperature <1000°C
- Scaled nickel silicide

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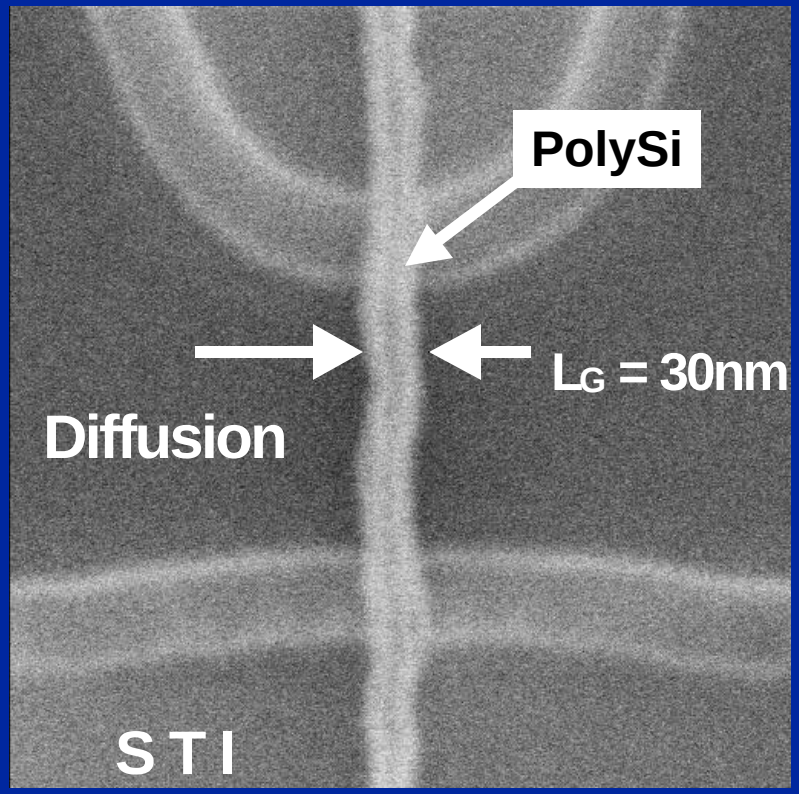
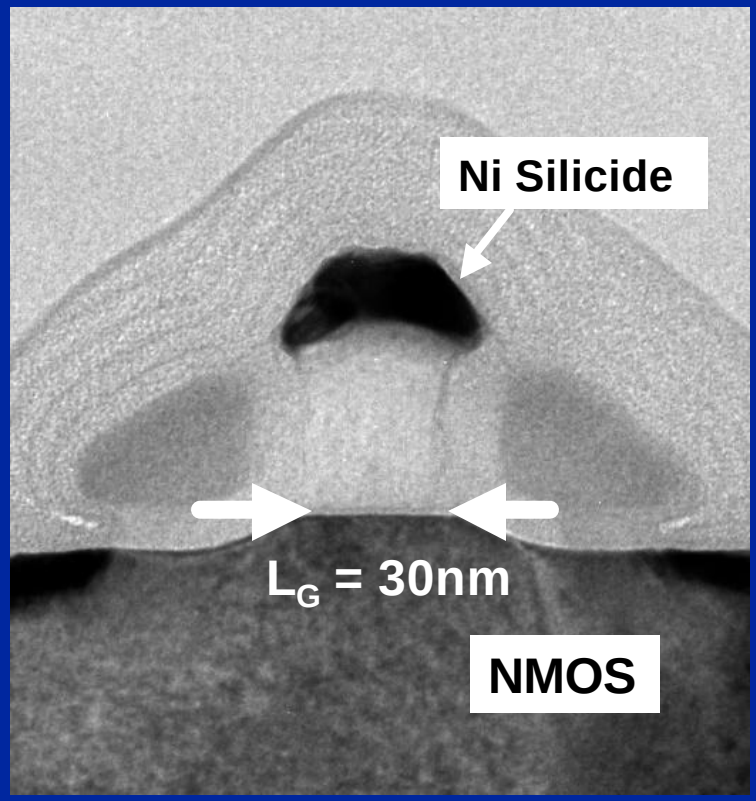
Research Transistor with 30nm Physical Gate Length





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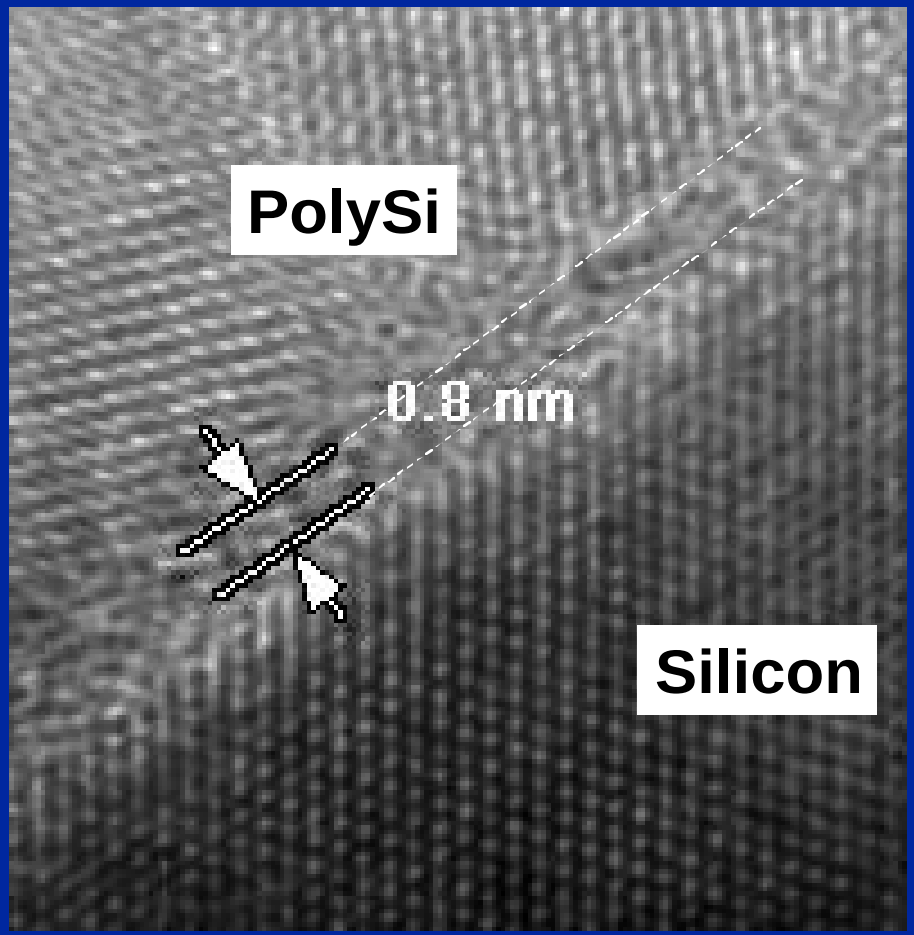
0.8nm Gate Oxide



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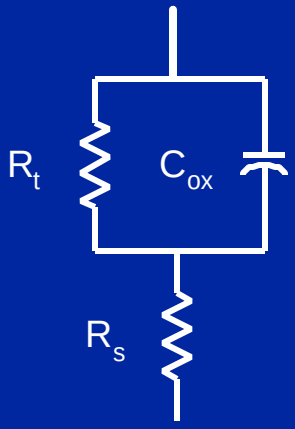
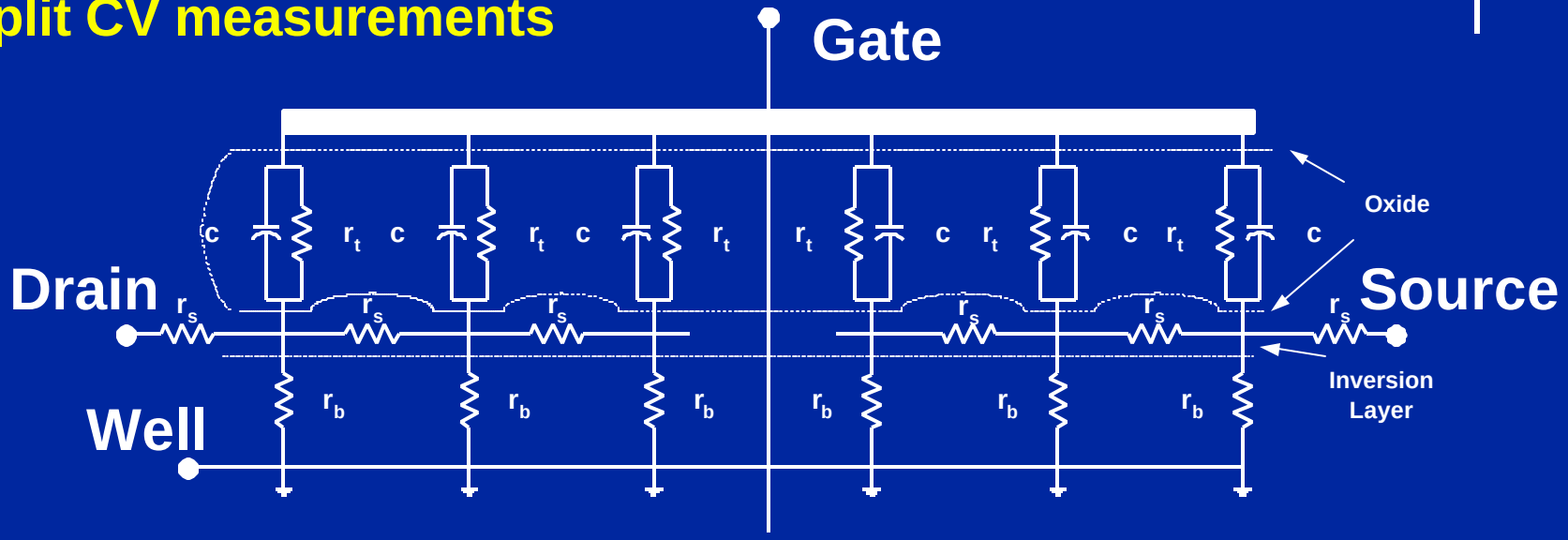
Transmission Line CV Methodology

- 3-element model not adequate for accurate capacitance extraction when gate leakage exceeds 20A/cm²
- Distributed transmission line model provides accurate device capacitance extraction from split CV measurements





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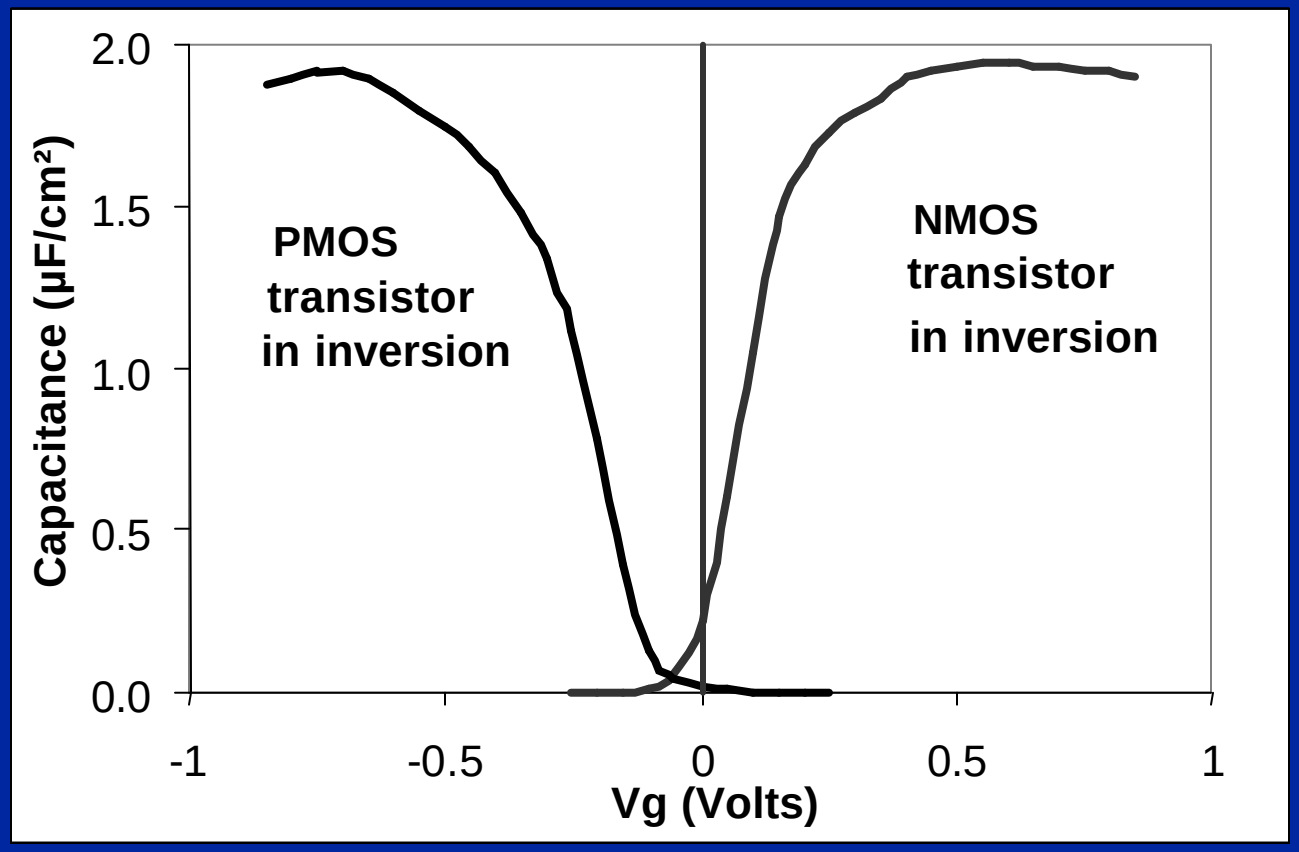
Transistor Gate Inversion Capacitance for 0.8nm Gate Oxide



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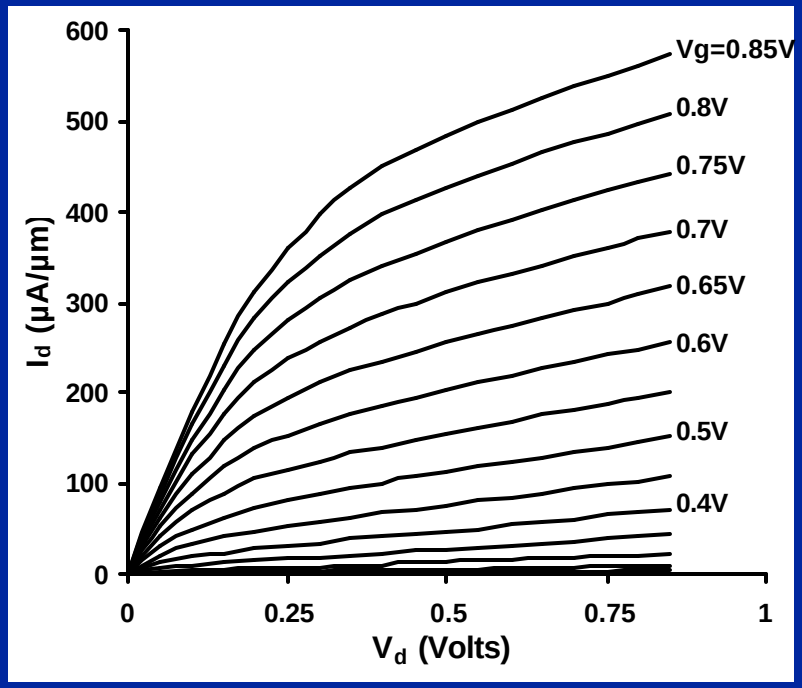
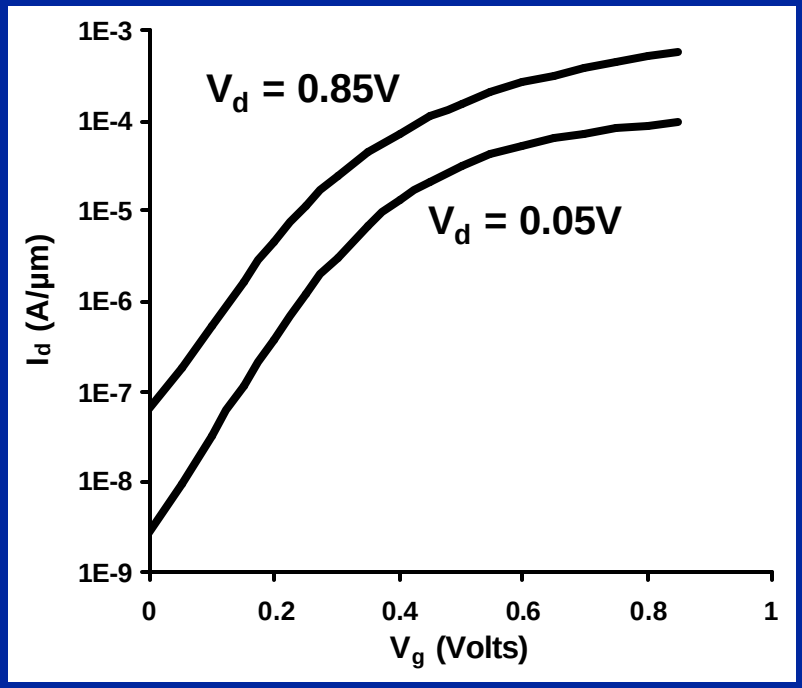
30nm L_G NMOS Transistor





- I_{on} = 0.57mA/µm, I_{off} = 60nA/µm at V_{DD} = 0.85V
- Subthreshold slope = 100mV/decade
- DIBL = 125mV/V

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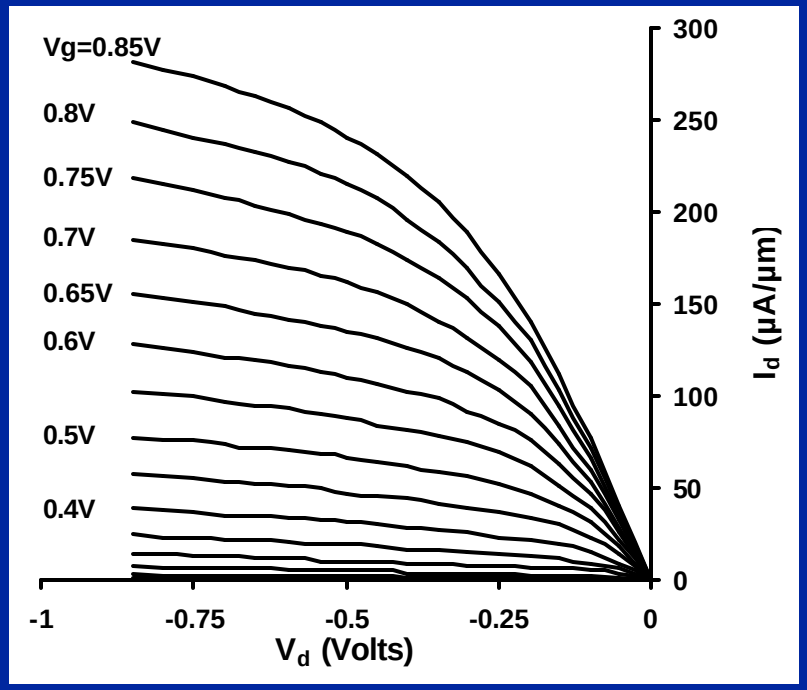
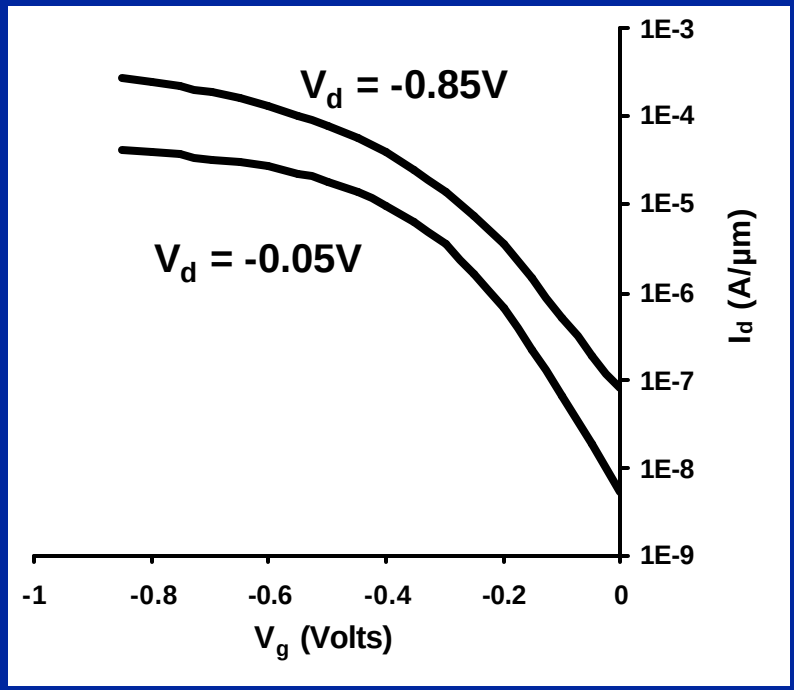
30nm L_G PMOS Transistor





- I_{on} = 0.28mA/㎜, I_{off} = 80nA/㎜ at V_{DD} = 0.85V
- Subthreshold slope = 100mV/decade
- DIBL = 125mV/V

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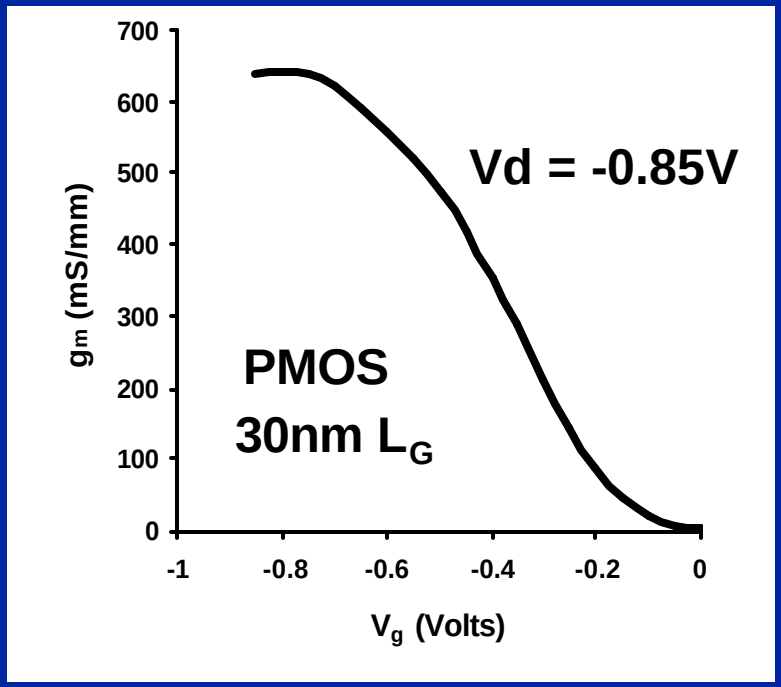
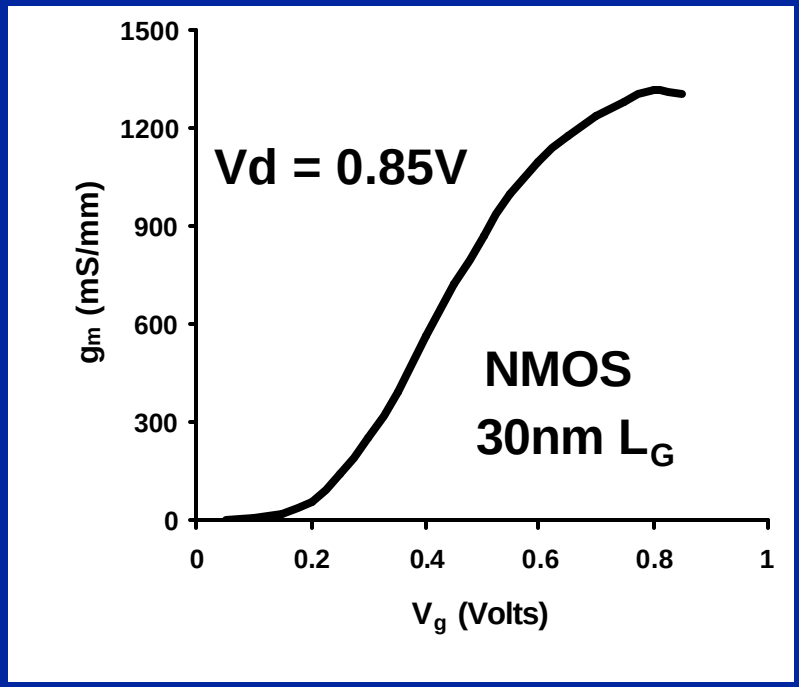
Transconductance





- Peak saturation gm for NMOS = 1300mS/mm
- Peak saturation gm for PMOS = 640mS/mm

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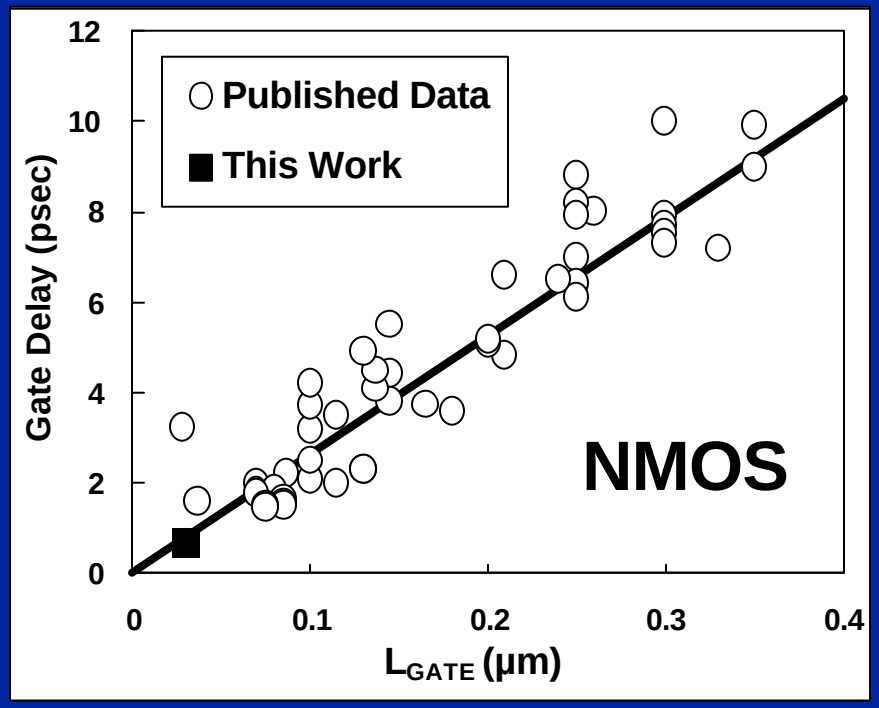
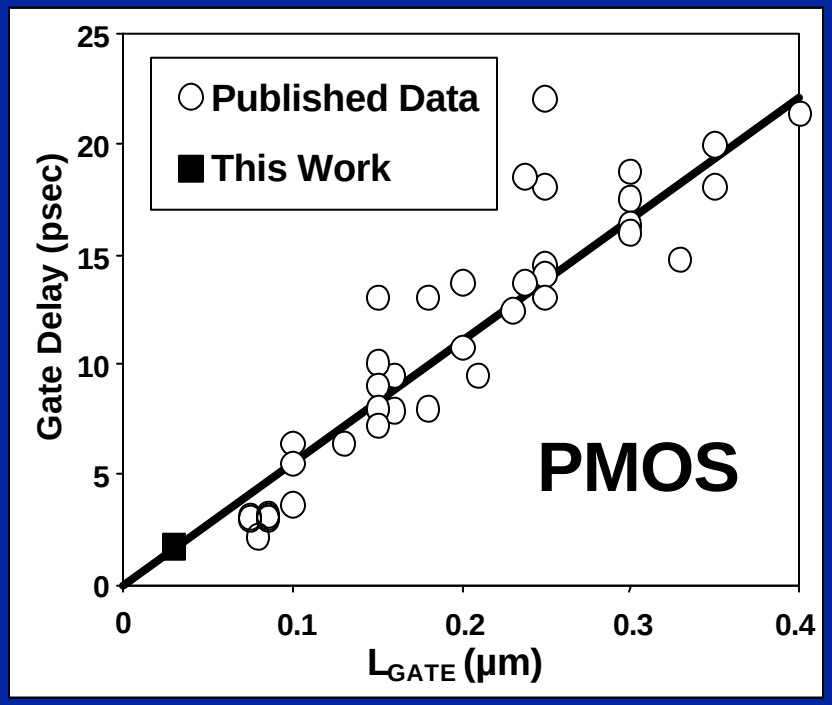
CV/I Gate Delays





- NMOS gate delay = 0.85ps, PMOS gate delay = 1.7ps
- Gate delays continue to follow historical trends

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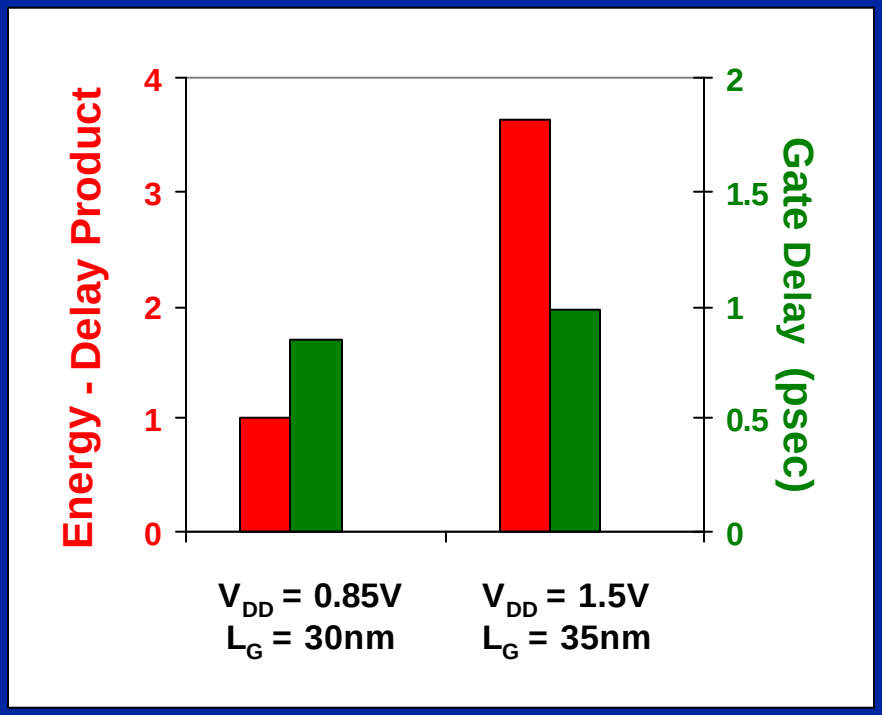
Importance of Low V_{DD}: Energy-Delay Product



Energy-Delay Product:

$CV^2 \times CV/I = C^2V^3/I$

- 35nm NMOS designed and fabricated for high V_{DD}
- 35nm NMOS @ 1.5V has >3.5X higher energy-delay product than 30nm NMOS @ 0.85V
- The choice of low V_{DD} (<1.0V) is necessary for the 70nm technology node

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Junction Edge Leakage (I_{JE})

- Parasitic tunneling reverse leakage current in transistor source and drain
- Increases with channel doping concentration
- Is I_{JE} a limiter for 70nm technology node where doping concentration approaches $4x10^{18}$ cm^{-3} ?

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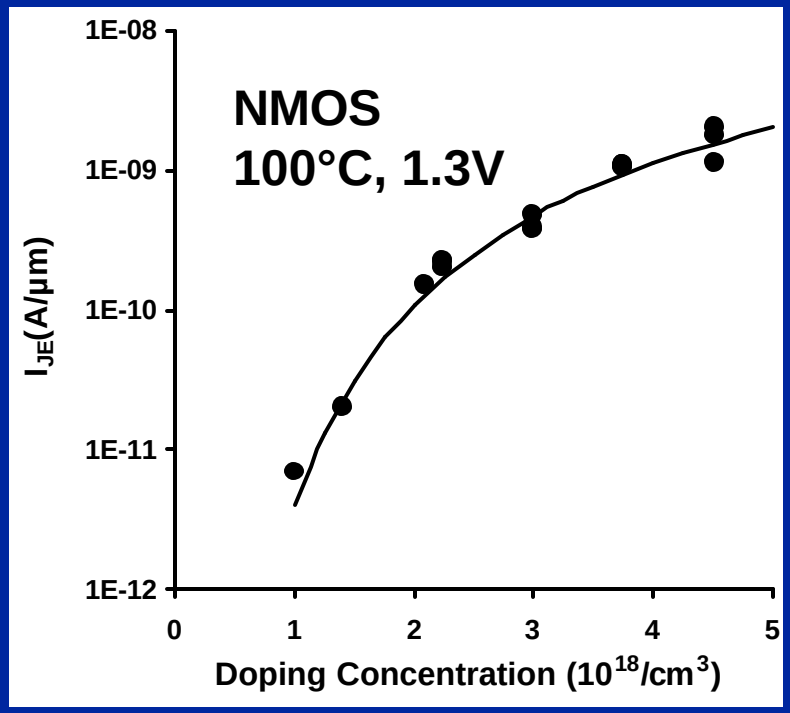
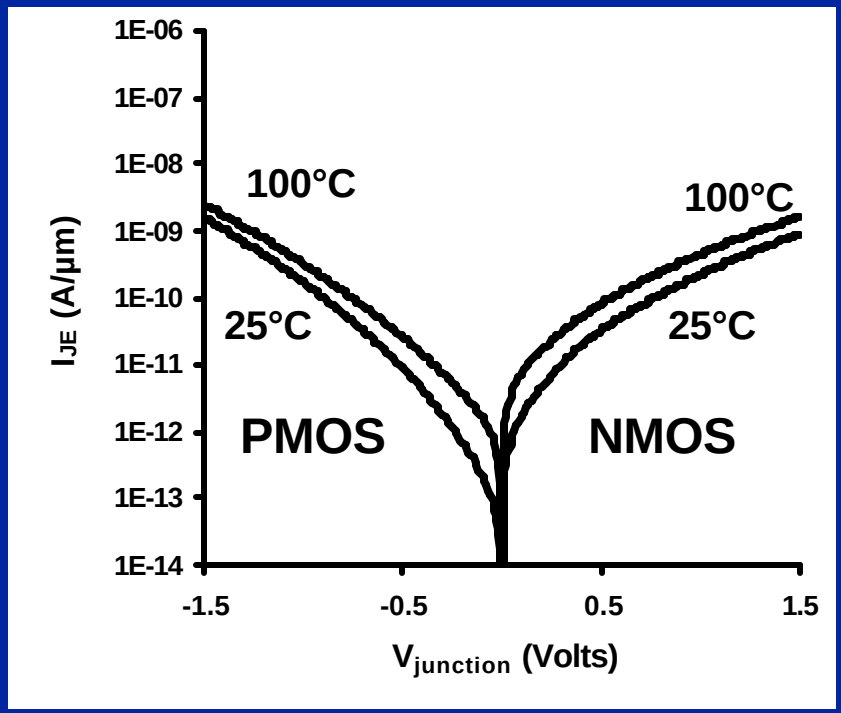
Junction Edge Leakage





- Junction edge leakage = ~1.0nA/um at 1.3V/100°C for channel doping = $4x10^{18}$ cm^{-3}
- Not a concern for the 70nm technology node

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Conclusions

- Conventional planar CMOS transistors with 30nm physical gate length show good short channel effect and device performance at V_{DD} = 0.85V
- Demonstrated the feasibility of high quality 0.8nm gate oxide
- Junction edge leakage not a concern for the 70nm technology node
- Planar CMOS transistors are scalable to the 70nm technology node, which will be in production 2005

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